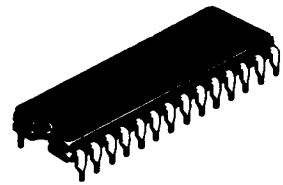
32768×8-bit or 65536×4-bit CMOS Mask Programmable Read Only Memory

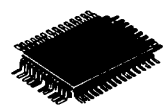
The Hitachi HN61256P/FP is a mask programmable 32768 x 8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

HN61256P



(DP-28)

HN61256FP

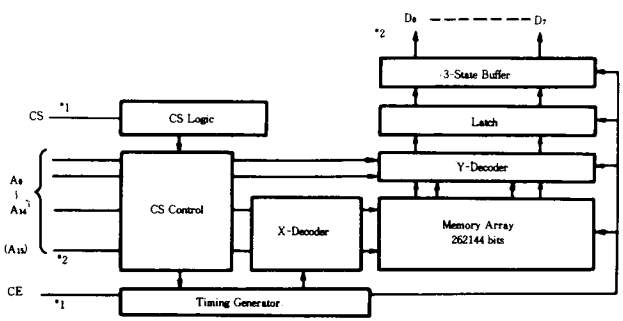


(FP-54)

■FEATURES

- Mask-programmable selection of either 4-bit or 8-bit organization
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply (±10%)
- Low power consumption: Operation 7.5mW (typ.), Standby 5μW (typ.)
- TTL compatible
- Access time: 3.5μs (max)

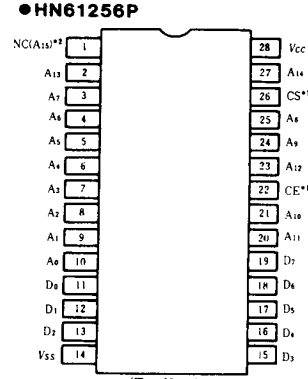
■BLOCK DIAGRAM



*1 Active level defined at mask level.
*2 Mask programmable selection of either 4-bit or 8-bit organization.
In 4-bit organization, data outputs are D_0 to D_3.

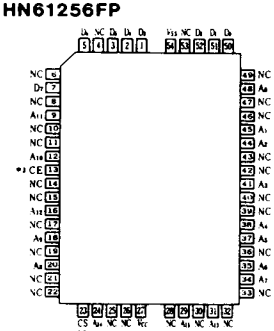
■PIN ARRANGEMENT

●HN61256P



(Top View)

●HN61256FP



(Top View)

*1. Active level defined by user
*2. Upper address of 4-bit organization.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{CC}	−0.3 ~ +7.0	V
All Input and output Voltage*	V_T	−0.3 ~ V_{CC}	V
Operating Temperature Range	T_{opr}	0 ~ +75	°C
Storage Temperature Range	T_{stg}	−55 ~ +125	°C
Bias Storage Temperature Range	T_{bias}	−20 ~ +85	°C

Note : * Referenced to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 ~ +75°C)

Item		Symbol	Test Conditions		min	typ**	max	Unit
Input "High" Level Voltage		V_{IH}			2.4	—	V_{CC}	V
Input "Low" Level Voltage		V_{IL}			0	—	0.8	V
Output "High" Level Voltage		V_{OH}	I_{OH} = −100 μA		2.4	—	—	V
Output "Low" Level Voltage		V_{OL}	I_{OL} = 1.6 mA		—	—	0.4	V
Input Leakage Current		I_{LI}	V_{in} = 0 ~ 5.5V		—	—	2.5	μA
Output "High" Level Leakage Current		I_{LOH}	$\overline{CE}$ = 0.8V	V_{out} = 2.4V	—	—	5	μA
Output "Low" Level Leakage Current		I_{LOL}	$\overline{CE}$ = 2.4V	V_{out} = 0.4V	—	—	5	μA
Supply Current	In stand-by	I_{SB}	$\overline{CS} \geq V_{CC}$ − 0.2V, $CS \leq$ 0.2V	V_{CC} = 5.5V	—	1	30	μA
	In operation	I_{CC}*	t_{RC} = 4.0 μs, I_{out} = 0mA, t_{CE} = 3.0 μs		—	1.5	3.0	mA
Input Capacitance		C_{in}***	V_{in} = 0V, f = 1MHz, Ta = 25°C		—	—	10	pF
Output Capacitance		C_{out}***			—	—	12.5	pF

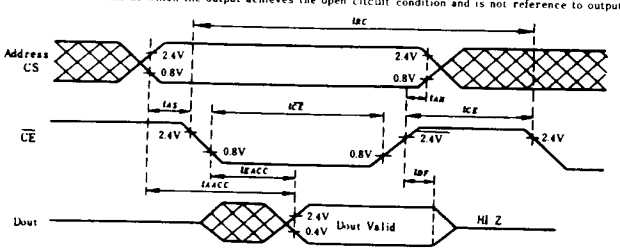
* Steady state current ** V_{CC} = 5V, T_a = 25°C
*** This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS

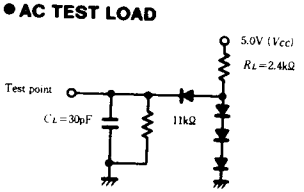
● READ CYCLE (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 ~ +75°C, $t_r = t_f$ = 20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	4.0	—	μs
Address Access Time	t_{AACC}	—	3.5	μs
Chip Enable Access Time	t_{EACC}	—	3.0	μs
Data Hold Time from Address	t_{DF}*	0.05	0.5	μs
Address Set-up Time	t_{AS}	0.5	—	μs
Address Hold Time	t_{AH}	0	—	μs
Chip Enable ON Time	$t_{\overline{CE}}$	3.0	—	μs
Chip Enable OFF Time	t_{CE}	0.5	—	μs

* t_{DF} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.



● AC TEST LOAD



Notes) 1. $t_r = t_f$ = 20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074(H).